



CADENCE AND IBM

IBM Accelerates Large-scale PCB System Design Using Unique Cadence Multi-style Design Entry Solution

“The Cadence solution enables us to enter up to 99 percent of signals in table format, which, along with improved analytics and a unique integrated environment, reduces our PCB development time by 80 percent.”

Gisbert Thomke, Group Leader, IBM R&D Lab Germany

IBM R&D LAB GERMANY

- One of the largest IBM labs outside of the U.S.
- Designs and builds large mainframe computers

BUSINESS CHALLENGE

- Shorten time-to-market for mainframe computer designs requiring highly complex PCB systems

DESIGN CHALLENGES

- World’s most complex PCBs
- Large designs, multiple wide buses
- High component pin counts and thousands of board connections

CADENCE SOLUTION

- Integrated platform—from input to final design
- Tabular input of signal information for faster compilations

CADENCE PRODUCTS

- Allegro System Architect GXL
- Allegro PCB Editor

PUSHING THE LIMITS OF PCB DESIGN

Mainframe computers provide speed and power unavailable in any other computing platform. In order to satisfy ever-increasing performance requirements, hardware design for mainframe components must constantly push the envelope of technology and complexity.

IBM has been the bellwether in mainframe computing for more than 50 years. Today, it continues to lead the way in large-scale design, creating mainframe computers that employ printed circuit boards (PCBs) measuring as large as 50cm x 60cm. Unlike bulky old-fashioned boards, these are enormous configurations of super-miniaturized components. A single board can carry tens of thousands of signal interconnects in more than 10 layers of circuitry. Adding to this complexity, pin counts reach 5,000 per component—with many

wide buses connecting them—while at the board level there may be more than 5,000 connections.

While these statistics are impressive, the design challenges that IBM faces are similar to those faced by any PCB designer. For example, once a circuit design involves hundreds of signals on a large bus, traditional schematics can be cumbersome and time-consuming to work with and analyze. IBM sought to simplify input and manipulation by developing its own solution based on entering the design attributes of each signal in a table or spreadsheet format. However, this created another step in the process—engineers then had to convert the information into Hardware Description Language (HDL) to interface with the design platform. IBM engineers also found they could not treat analog elements in this way; they still had to configure them manually.

When the engineers at IBM R&D Lab Germany learned that Cadence had developed an integrated solution that managed both tabular and schematic data in a full design and simulation environment, they adopted Cadence® Allegro® System Architect GXL.

“Now we can use one design system globally to speed design iterations—even those spanning from the logical system design to the physical implementation of the system—with speed and accuracy. Allegro System Architect is the only product we have found that offers a totally integrated design system,” explained Gisbert Thomke, PCB group leader at the IBM R&D Lab Germany.

THE BENEFITS OF SPEEDY INPUT AND FASTER COMPILES

The primary reason the German IBM lab adopted the Cadence solution is that it enables designers to enter and manipulate signal specifications as easily as with an accounting spreadsheet. Design teams using the tabular input capability of Allegro System Architect can complete the input in one-tenth of the time required to work directly with schematics, and with fewer errors. Using this method, designers can also output charts and tables that provide much better analysis for constraint management.

Thomke stressed the importance of this holistic approach: “This Cadence solution provides us with a far more comprehensive view of the system structure and greater visibility of the buses. It allows us to forecast the number of layers that will be required. This is critical for us, because we are working at the edge of what manufacturing can produce.”

Another major benefit of Allegro System Architect is that compiling the design code takes a fraction of time previously required for schematics. The German experts were typically dealing with compilation times in the 8 to 10 hour range, so compiling

could only be performed once a day—usually overnight—and produced up to 400 pages of printout to check. Consequently, a simple typographic mistake could mean the loss of an entire day in the schedule.

Now, using Allegro System Architect, the IBM development team can complete compilation in a matter of seconds. This speed enables engineers to perform incremental compiles for a smaller number of changes, providing quick detection of errors and radically increasing efficiency and productivity. Rapid compilations also translate into two additional benefits: 1) companies can meet or beat project schedules; and, 2) design teams can use the time gained to explore design alternatives, reducing the cost of experimentation and innovation, and resulting in the best possible design. Thomke summarized the difference: “We used to go through 40 to 50 design iterations over the entire development cycle. Now we can run that many in a couple of days.”

SOLVING TOUGH PROBLEMS WITHIN TIGHT TIMELINES

Finding innovative solutions to difficult problems without jeopardizing project schedules is a key challenge when teams are pushing the limits of functionality and designing at the edge of manufacturability. The tabular input method is a good example of how the IBM lab continually develops a variety of methods to improve its design process. However, they quickly bumped up against the limitations of this innovation: analog signals still required schematic input, for example, so the two systems of input had to be merged by yet another process.

Once the IBM R&D lab in Germany verified that Allegro System Architect GXL could meet all of its requirements in a single integrated software package from beginning to end, it adopted Cadence as its dedicated design platform for all PCB development. The integrated environment allows engineers to assess


more quickly and easily how front-end definitions will affect back-end design issues. Overall, the improved entry, analytics, and integration have reduced the time required for PCB development by 80 percent. These savings were then re-invested in functionality and quality improvements.

SUCCESS DRIVES USE BEYOND EARLY ADOPTERS

The IBM R&D Lab Germany PCB group has now developed several boards, including some very large designs with many wide buses using Allegro System Architect software. The German group's experience has been so positive that now other divisions of IBM around the world are also moving to Allegro System Architect for their PCB designs.

Adoption of the new design environment was smooth thanks to FlowCAD, a Cadence Channel Partner, which provided valuable support to IBM R&D Lab Germany. “There was always a quick response from the FlowCAD engineers, and we had many very useful discussions that helped us to improve both our design and methodology,” added Thomke. The Cadence R&D group also directly provided a number of accelerated responses and enhancements to IBM's unique requirements.

In summarizing this partnership, Thomke affirmed that, “We are proud to be on the absolute leading edge of PCB technology in terms of size and complexity—with data volumes in the range of 80MB to 400MB—and we are pleased that Cadence is there with solutions that give us the performance advantage to keep moving forward.”



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